Quantum Interference in Silicon 1D Junctionless Nanowire Field-Effect Transistors

F. J. Schupp[1], Muhammad M. Mirza[2], Donald A. MacLaren[3],
G. Andrew D. Briggs[1], Douglas J. Paul[2], and Jan A. Mol[1*]
[1] *University of Oxford, Department of Materials, 16 Parks Road, Oxford OX1 3PH, UK*
[2] *University of Glasgow, School of Engineering, Rankine Building, Oakfield Avenue, Glasgow, G12 8LT, United Kingdom*
[3] *University of Glasgow, SUPA School of Physics and Astronomy, Kelvin Building, University Avenue, Glasgow, G12 8QQ, United Kingdom*
(Dated: December 5, 2018)

We investigate the low-temperature transport in 8 nm diameter Si junctionless nanowire field-effect transistors fabricated by top down techniques with a wrap-around gate and two different phosphorus doping concentrations. First we extract the intrinsic gate capacitance of the device geometry from a device that demonstrates Coulomb blockade at 12 mK with over 500 Coulomb peaks across a gate-voltage range of 6 V indicating the formation of an island in the entire 150 nm-long nanowire channel. In two other devices, made from silicon on insulator wafers that were doped to an activated dopant concentration of Si:P $4 \times 10^{19}\,\mathrm{cm}^{-3}$ and $2 \times 10^{20}\,\mathrm{cm}^{-3}$, we observe quantum interference and use the extracted gate coupling to determine the mean-free paths from the dominant energy scale on the gate-voltage axis. For the higher doped device the analysis yields a mean-free-path of $4 \pm 2\,\mathrm{nm}$, which is on the order of the average spacing of phosphorous atoms and suggests scattering on unactivated or activated dopants. For the device with an implanted phosphorous density of $4 \times 10^{19}\,\mathrm{cm}^{-3}$ the quantum interference effects suggest a mean-free-path of $10 \pm 2\,\mathrm{nm}$, which is comparable to the nanowire width, and thus allows for coherent formation of transversal modes. The results suggest that the low-temperature mobility is limited by scattering on phosphorus dopants rather than the expected surface roughness scattering for nanowires with diameters larger or comparable to the Fermi wavelength. A temperature dependent analysis of Universal Conductance Fluctuations indicates a phase-coherence length greater than the nanowire length for temperatures below 1.9 K and decoherence from 1D electron-electron interactions dominates transport for higher temperatures. Our measurements therefore provide insight into scattering and dephasing mechanisms in technologically relevant silicon device geometries, which will help with future design choices with regards to e.g. doping density.

I. INTRODUCTION

Silicon nanowires have been extensively studied with diameters down to below 5 nm[1,2] and for a wide range of applications including electronics[3,4], qubits[5], biosensors[6,7], colour-selective photodetectors[8], photovoltaics[9] and thermoelectric generators[10]. Short-channel effects and poor electrostatic control of the channel in two-dimensional transistors, such as MOSFETs, have led to significant work on nanowire transistors. In these devices, a wrap around or Omega gate provides strong electrostatic control of the channel[11] and electron transport can become one-dimensional (1D) for small nanowire-diameters[12]. Technological applications of nanowires require identification and control of the dominant scattering processes to ensure reproducibility and sufficient carrier mobility. These aspects need to be considered in the context of 1D transport, that has been studied extensively in carbon-nanotubes, metal- and semiconductor-nanowires[13–17]. Strong radial confinement in these systems leads to the formation of subbands, that can be populated or depleted with excellent electrostatic control in e.g. multi-gate geometries. In ultra clean devices, with scattering lengths longer than the one-dimensional transport channel, quantum interference leads to Fabry-Perot-type transport where energy is only dissipated at the source and drain contacts[18]. The short channels required for such devices are challenging to realize with different doped regions, such that a homogeneously doped "junctionless" design is a promising candidate if scattering in the channel can be minimized[4]. Here we demonstrate gate all-around junctionless silicon-nanowires, that were fabricated from silicon-on-insulator wafers with an activated Si:P concentration of $4 \times 10^{19}\,\mathrm{cm}^{-3}$ and reach a mean-free-path larger than the diameter. The dominant scattering process can be linked to doping concentration rather than surface roughness scattering or interface traps from e.g. trapped charges at the material interfaces of the gate oxide. This is the result of high doping densities, highly optimized fabrication and low interface trapped-charge density.

II. NANOWIRE CHARACTERISTICS

We have investigated P doped Si nanowires with a length of $L = 150$ nm and a wrap-around aluminium gate that surrounds the entire nanowire (for fabrication details see Supplementary Information[19]). The physical parameters of the silicon nanowire, such as diameter, length, crystallinity, and interface quality are crucial in determining its transport properties. We therefore

characterize the fabrication process using an electron-energy-loss spectroscopy scanning-transmission-electron micrograph (EELS-STEM) and capacitance-voltage (C-V) measurements. Figure 1a shows a top-view scanning-electron microscope (SEM) image of the device structure. Although the gate covers the channel as well as a part of the source and drain contacts, the transport is dominated only by the nanowire channel since larger 3D structures cannot be controlled by the gate. This was shown in previous work, where the conductivity in the nanowires could only be well controlled for 1D transport, if the Fermi wavelength λ_F is larger than the nanowire diameter d ($\lambda_F > d$). For larger diameters where $\lambda_F < d$, the channel conductivity could not be controlled by the gate electrode as the nanowires became 3D for electron transport and therefore screened the electric field on the nanowire surface[12,20]. A high resolution STEM image in Fig. 1b, with the [111] and [220] lattice fringes highlighted in red, confirms that the Si is a single-crystal lattice oriented along [110] and surrounded by the amorphous SiO_2. Figure 1c is an EELS-STEM image of the cross-section of a nanowire transistor with an inner diameter of 8 ± 0.5 nm, as determined from the transition in relative Si and O concentrations presented in Fig. 1d. The EELS-STEM data shows that the gate is not perfectly wrapped around the nanowire resulting in a vacuum-gap underneath a section of the gate oxide. The previously reported on-current to off-current ratio above 10^8 with subthreshold slope of 66 mV/dec at 300 K demonstrates that this gap does not significantly affect the electrostatic control of the channel by the gate[12,20]. We will confirm the effectiveness of the wrap-around gate at 12 mK by analyzing the gate capacitance based on the electron addition energy below.

Another factor that impacts the nanowire transistor performance is the quality of the surface passivation. In the supplementary information[19], we investigate the role of deep interface-trapped states using C-V characteristics of 100 μm circular MOS capacitors fabricated with 10 nm thermally grown SiO_2 that were processed in the same oxidation furnace in which the nanowires were produced. The measurement demonstrates that the key process is a forming gas anneal that passivates the dangling bonds and trapped charges with hydrogen atoms, such that the interface-trap density D_{it} can be lowered by over an order of magnitude down to 1.3×10^{10} cm^{-2} eV^{-1} – this corresponds to less than one trap per nanowire on average.

III. MEASUREMENTS

In the following we characterize the transport through our devices using two types of measurements that both employ battery-powered DC measurement-electronics to apply gate- and bias-voltages. For the temperature dependence in Fig. 3 we use a lock-in technique at a frequency of 1337.3 Hz with an excitation amplitude of 50 μV for temperatures below 1.45 K and 100 μV for higher temperatures. All other measurements were carried out in DC using a current amplifier that is also powered by a battery. The measurement system was carefully filtered to ensure low electron-temperatures and the associated series resistance was calibrated out of the data. With exception of the conductance in Fig. 3, that is measured directly with a lock-in amplifier, all conductance and transconductance data are calculated from numerical derivatives of the measured current.

A. Coulomb blockade regime

Fig. 2 presents data from device A – a 8 ± 0.5 nm diameter nanowire with a 150 nm channel made from a wafer with an activated P concentration of 2×10^{20} cm^{-3}. The device shows signatures of single-electron transport at 12 mK with more than 500 evenly spaced Coulomb peaks over a large gate-voltage range from -4.5 to +2 V. Figure 2a shows a small fraction of these features in current and the full gate-voltage range is presented in the Supplementary Information[19].

To characterize the peak-spacing over the entire gate-voltage range, we calculate the autocorrelation function $R_{xx} = \int I(V_g)I(V_g - \Delta V_g)\mathrm{d}V_g$ of the current as a function of gate-voltage in Fig. 2b. The autocorrelation demonstrates oscillations that correspond to a spacing of the Coulomb blockade peaks $\Delta V_{CB} = 10 \pm 2$ mV. The overall decrease in the autocorrelation is related to effects on a larger gate-voltage scale, such as the larger scale fluctuations in the Coulomb peak height (as shown in the Supplementary Information[19]). Alternatively there is a histogram shown in the Supplementary Information[19]. In Fig. 2c we show the corresponding Coulomb diamonds in conductance G as a function of gate-voltage V_g and bias-voltage V_b.

The regular spacing of the Coulomb blockade peaks indicates that the charge island has a fixed capacitance, and therefore a fixed size, which implies that an island forms within the channel that is defined by two tunnel barriers and persists over a large gate-voltage range. We estimate the island length by comparing the capacitance to the gate C_g taken from the data to a theoretical value that follows from a simple cylindrical-capacitor model (see Supplementary Information[19]). The model for a 150 nm nanowire yields $C_g = 15.2$ aF, while the capacitance from the data in Fig. 2 is extracted from the spacing on the gate-voltage axis at zero bias $\Delta V_{CB} = 10 \pm 2$ mV[21]:

$$C_g = e/\Delta V_{CB} = 16 \pm 4\,\mathrm{aF} \quad (1)$$

where e is the elementary charge.

From the good agreement of the experimental and theoretical values for the capacitance, we conclude that

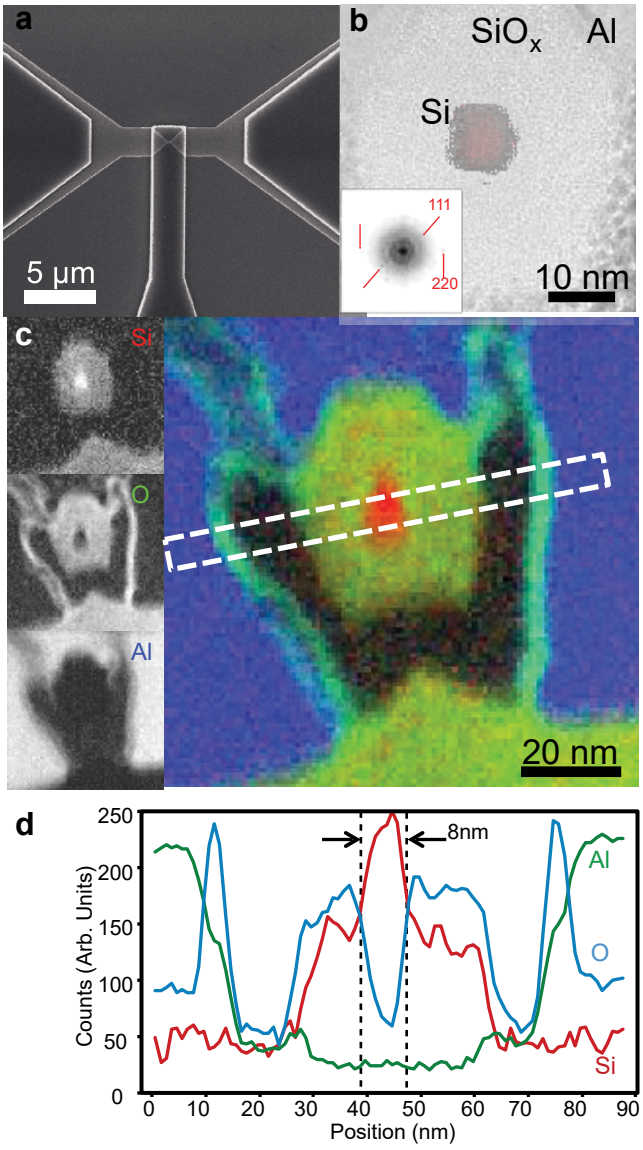

FIG. 1. a) Top view of the device taken using a SEM. b) Cross-sectional TEM image of nanowire with the lattice fringes picked out in red using a filtered Fourier transform (inset) to select lattice fringes. c) Elemental mapping of the same nanowire. The main image is a composite of silicon (red), oxygen (green) and aluminium (blue) signals with the individual maps inset to the left. d) Integrated signal intensity profiles across the dashed region of the RGB map used to determine the wire width.

the tunnel barriers are located close to the ends of the nanowire channel, i.e. the charge island has the same length as the nanowire. The extracted value of the capacitance is intrinsic to the nanowire geometry and therefore valid for all geometrically identical devices. The formation of tunnel barriers at the ends of the channel are either related to nanowire thickness variations from e.g. proximity effects in lithography, strain and/or the accumulation of impurities[22]. Device A is the only tested

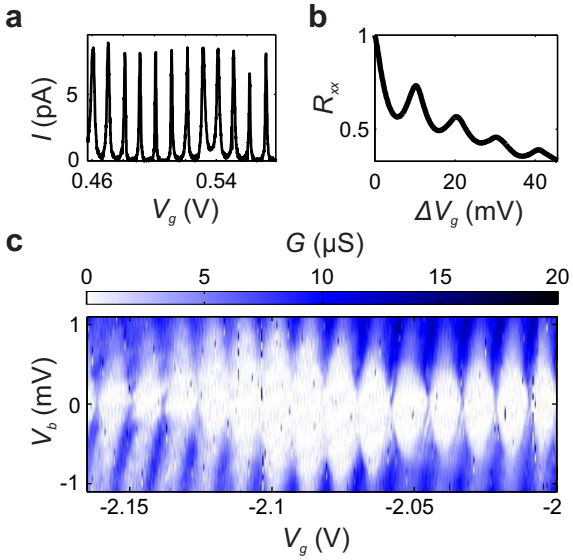

FIG. 2. Coulomb blockade data from device A: a) Current I at 0.1 mV bias as a function of gate-voltage V_g. b) Normalized autocorrelation function R_{xx} of the current in a larger gate-voltage window from -4.5 V to +2 V. c) Conductance G as a function of gate-voltage V_g and bias-voltage V_b.

device displaying a Coulomb blockade regime over a large gate-voltage range and the channel does not become more conductive at larger gate voltages as observed in device B and C. This behavior was observed only in device A, which is on the same chip as device C. It is therefore unlikely that the associated tunnel barriers arise from a systematic error in the lithography. Instead a local effect from e.g. charging impurities could have affected the fabrication process.

B. Quantum interference regime: temperature dependence

We now turn to measurements on device B, that, unlike device A, shows a high-conductance regime similar to all other measured devices. Transport data from measurements on device B are shown in Fig. 3, 4 and 5a,b. Device A and B are geometrically identical, with 150 nm channel length and 8 ± 0.5 nm diameter, but device B was fabricated from a wafer with a lower activated phosphorus-doping-concentration of $4 \times 10^{19}\,\mathrm{cm}^{-3}$. While the low-temperature conductance data do not show the regular Coulomb blockade pattern over a large gate-voltage range as in device A, there are some Coulomb peaks at low gate-voltages. The associated Coulomb diamonds strongly vary in size (see Supplementary Information[19]) and often do not close completely, which is a signature of transport through one or more islands in the nanowire with varying sizes as a function of gate-voltage. It is therefore likely that the charge islands form as a result of potential variations

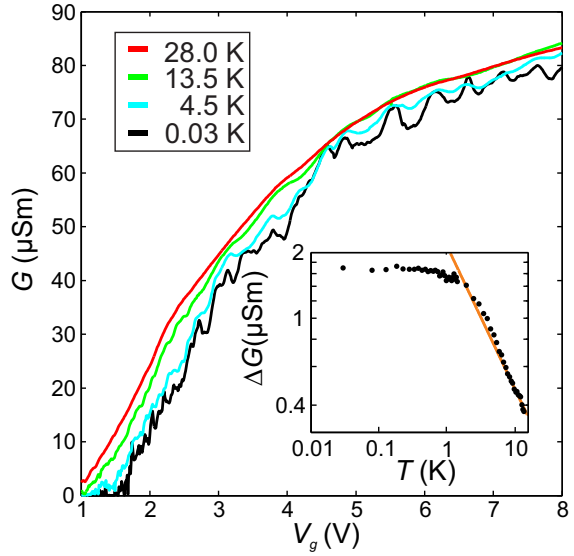

FIG. 3. Temperature dependent conductance in device B: a) Conductance G as a function of gate-voltage V_g at four different temperatures from 30 mK to 28 K (Temperature traces at 82 temperatures are shown in the Supplementary Information[19]). Inset: Root-mean square of the conductance traces ΔG after subtracting a fourth degree polynomial fit to isolate the fluctuations from the background as a function of temperature T. The red line is a fit with $\Delta G \propto T^{-\gamma}$ resulting in $\gamma = 0.67 \pm 0.04$.

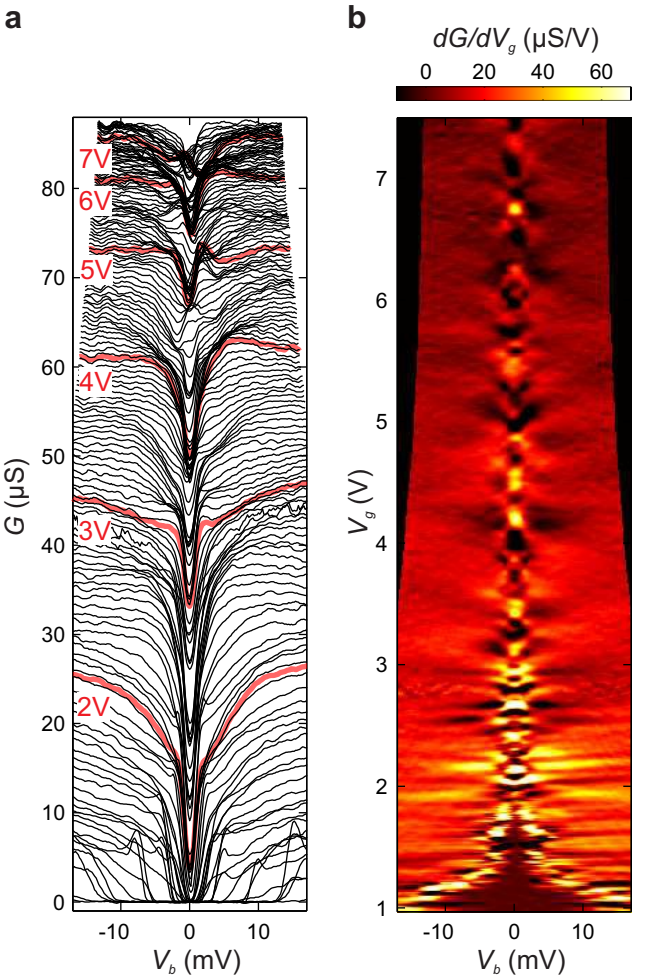

FIG. 4. Conductance fluctuations in device B (corrected for a series resistance of 13.5 kΩ): a) Conductance traces as a function of bias-voltage V_b at gate-voltages from 0.97 V to 7.5 V. The red lines indicate the traces at 2, 3, 4, 5, 6, and 7 V gate-voltage. b) Transconductance dG/dV_g as a function of bias-voltage V_b and gate-voltage V_g.

along the nanowire and not solely due to potential barriers at the ends of the nanowire.

Transport in device A is dominated by Coulomb blockade over the entire presented gate-voltage window and does not display significantly increased conductance as expected for an opening channel at larger gate-voltages $V_g > 2$ V. Device B on the other hand is characterized by a Coulomb blockade region followed by increasing conductance without blockade at gate-voltages $V_g > 1.7$ V (see Supplementary Information[19]). Above this threshold-voltage we observe fluctuations in the conductance that we attribute to quantum interference effects that are analyzed in the next sections.

Quantum interference in nanoelectronics is the interference of partial charge-carrier waves such as the counter-propagating partial waves between two reflecting points. The required coherent scattering can occur on any stationary boundary such as the ends of the nanowire (longitudinal Fabry-Pérot type interference)[23,24], random potential fluctuations in the nanowire from e.g. impurities (Universal Conductance Fluctuations)[25,26] or transverse modes due to the confinement in the cross section of the nanowire (subbands or transverse Fabry-Pérot modes)[27]. In all of these cases constructive interference occurs at a series of resonant wavelengths and the resulting localization of the charge carriers manifests in reduced conductance. The charge carrier wavelength can be manipulated by bias-voltage or gate-voltage, such that quantum interference can be directly observed when measuring the conductance as a function of gate-voltage and bias-voltage.

Fig. 3 shows the conductance G at different temperatures from 30 mK to 28 K in device B as a function of gate-voltage V_g with a small Coulomb blockade region at low gate-voltage and oscillations from quantum interference for a more open channel. The amplitude of the quantum interference features is decreasing as the temperature is increasing until the G-V_g trace is nearly smooth at 28 K. In a conducting channel without averaging over independently fluctuating segments Universal Conductance Fluctuations are expected to reach amplitudes $\alpha e^2/h$ with $e^2/h = 38.7\mu$S and α on the order of 1 depending on device geometry[27,28]. In our data the largest fluctuation produces only $\alpha = 0.12$ which could be related to an unaccounted series resistance and/or reflections at the intersection of the bulk-like leads and the 1D channel.

The inset of Fig. 3 shows the root-mean-square of the G-V_g traces ΔG as a function of temperature after removing the background (the procedure for obtaining ΔG is described in the Supplementary Information[19]). Below 1.9 K ΔG does not depend on temperature, as predicted for the transport regime where the phase-coherence length l_ϕ is longer than the nanowire, such that there is no averaging over independently fluctuating segments of the nanowire[28]. For temperatures above 1.9 K the conductance fluctuations follow a power law $\Delta G \propto T^\gamma$ (see Supplementary Information[19])[27,29]. We can calculate the expected value for γ assuming that the phase-coherence length is proportional to $T^{-1/3}$, which is the case for a dominant dephasing mechanism related to 1D electron-electron interactions[29]. If the thermal broadening of the electron energy distribution, that is parameterized by the thermal length l_T, is larger (smaller) than the phase-coherence length, we then expect $\gamma = -2/3$ ($\gamma = -1/2$). For temperatures above 1.9 K, a power-law fit to our data with γ as a free parameter yields $\gamma = -0.67 \pm 0.04$ in excellent agreement with the case $l_T < l_\phi$.

C. Quantum interference regime: mean-free-path

Next we turn to conductance data as a function of gate- and bias-voltage to investigate the energy scales related to quantum interference and analyze the periodicity on the gate-voltage axis. Figure 4a shows the conductance G as a function of bias-voltage V_b for gate-voltages from 0.97 V to 7.5 V. The red lines mark the traces at 2, 3, 4, 5, 6 and 7 V in gate-voltage for clarity. All conductance traces show a dip centered around zero-bias that is typical for 1D systems[12,30,31]. In previous work we have related this feature to strong localization and electron-electron interactions[12].

In case there is only a little change in the conductance as a function of gate-voltage the lines in Fig. 4a are close together and the plot appears dark. Away from the Coulomb-blockade region, darker regions in this type of plot have been related to quantum interference and are expected to show a characteristic pattern of alternating zero-bias and non-zero bias features[14]. The zero-bias features correspond to a resonance with the Fermi energy of the charge carriers, while the non-zero bias features correspond to the point where the bias window encompasses the energies of a neighboring resonance. This results in a distorted diamond pattern, which can partly be observed in Fig. 4a between 5 and 6 V in gate-voltage as well as between 6 and 7 V. In that gate-voltage region as well as at lower gate-voltages other non-zero bias features are faint or not visible, such that the pattern cannot be seen. To visualise the conductance oscillations due to quantum interference in a different way, we show the transconductance dG/dV_g as a function of gate-voltage V_g and bias-voltage V_b in Fig. 4b. For lower gate-voltages ($V_g \lesssim 1.7$ V) we observe a gap in the conductance as a function of bias-voltage and some Coulomb blockade features that correspond to multiple charge islands in series (see Supplementary Information[19]). At higher gate-voltages, when the overall conductance increases (see Fig. 4a), quantum interference results in diamond shaped patterns as a function of gate- and bias-voltage in agreement with the faint distorted diamond pattern in Fig. 4a and the pronounced dark features around zero-bias.

In the remainder of this letter we will analyze the characteristic energy spacings of the conductance fluctuation pattern to infer the microscopic origin of the quantum interference and find the elastic mean-free-path l_e. To determine different transport regimes, we employ the definitions introduced by Beenakker and van Houten[27,32]. In the diffusive transport regime the wire diameter d as well as the length L are much larger than the elastic mean-free-path. In this regime there are many scattering sites in the channel, but effects of quantum interference can still modify the conductivity of the disordered conductor because elastic impurity-scattering does not destroy phase coherence. Transport is considered to be ballistic when the dimensions of the wire are reduced below the mean free path. The intermediate regime is characterized by $d < l_e < L$, meaning boundary-scattering and internal impurity-scattering are of equal importance. At low temperatures the phase-coherence length l_ϕ can extend over a large part of the wire and exceed L, resulting in conductance fluctuations when the transport is in the intermediate regime or even diffusive. By comparing the elastic mean-free-path to the sample dimensions we will determine whether the quantum interference is dominated by boundary-scattering or impurity-scattering.

We analyze the energy spacings of the conductance fluctuations in two different devices with length 150 nm and diameter 8 nm: device B (from the last sections), that was fabricated from a wafer with an activated phosphorus-doping-concentration of $4 \times 10^{19}\,\mathrm{cm}^{-3}$, and device C, where the activated phosphorus-doping-concentration of the wafer was $2 \times 10^{20}\,\mathrm{cm}^{-3}$. Figure 5a shows the transconductance dG/dV_g as a function of gate-voltage V_g and bias-voltage V_b for device B at 12 mK, while Fig. 5b shows the transconductance for device C at 4 K. To extract the energy scales we calculate the autocorrelation function of both data sets and take the Fourier transform to find the dominant voltage spacings between the fluctuations[33]. While the data can contain other periodicities, the strongest signal corresponds to the energy scale that is related to the dominant length of interference paths
and therefore to the mean-free-path. The result for device B is plotted in Fig. 5c and shows four symmetric hotspots (circled in white) corresponding to a gate-voltage spacing $\Delta V_g = 0.6 \pm 0.1\,\mathrm{V}$ and bias-voltage spacing $\Delta V_b = 30 \pm 26\,\mathrm{mV}$. For device C the same analysis in Fig. 5d shows hotspots corresponding to $\Delta V_g = 1.5 \pm 0.2\,\mathrm{V}$ and $\Delta V_b = 50 \pm 30\,\mathrm{mV}$. The extracted gate-voltage spacings from the two samples reflect the different

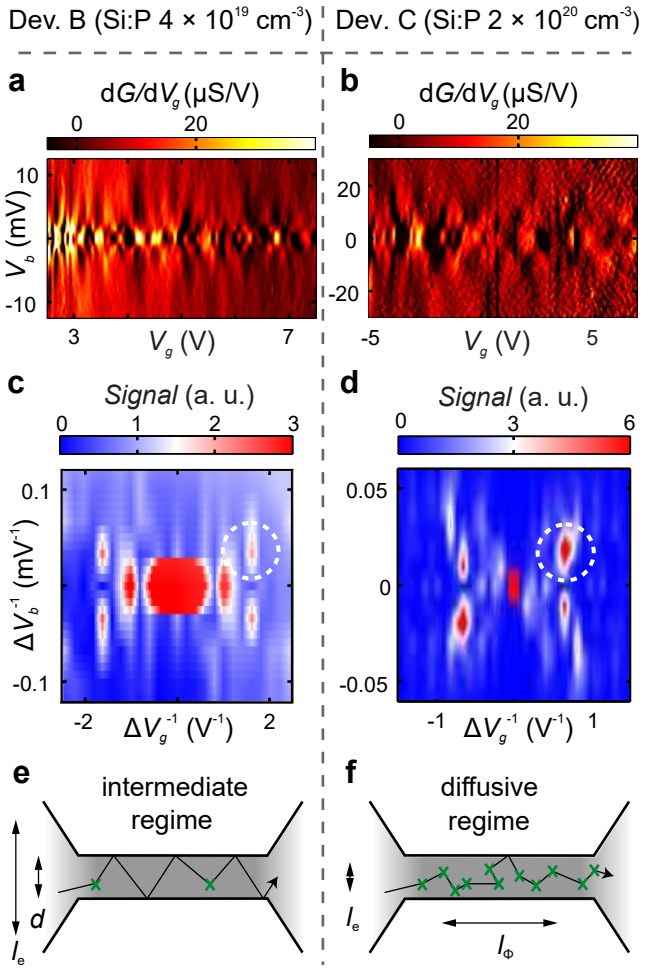

FIG. 5. Data from device B at 12 mK: a) Transconductance dG/dV_g as a function of gate-voltage V_g and bias-voltage V_b, c) Fourier transform of the autocorrelation of the data in a) with one of four symmetric hotspot circled in white. Data from device C at 4 K: b) Transconductance dG/dV_g as a function of gate-voltage V_g and bias-voltage V_b, d) Fourier transform of the autocorrelation from c) with a hotspots circled in white. e) Schematic depiction of a typical electron-path through a nanowire with diameter d and length L in the intermediate transport regime. Relatively few scattering events (denoted by the green markers) allow for standing wave modes in the circular nanowire cross-section. f) Schematic depiction of a typical electron path through a nanowire in the diffusive transport regime. Unlike in Fig. 5e, scattering is so frequent that there are no standing wave modes that are only bound by the nanowire walls.

energy spacings in the corresponding transconductance plots Fig. 5a,b. Since there is no repeating pattern along the bias-voltage axis in Fig. 4, the periodicity in bias-voltage does not give an accurate picture of the energy spacings and is likely related to artefacts from the limited bias-voltage range of the data.

To identify the origin of the conductance fluctuations from quantum interference, we convert the extracted gate-voltage spacings into the characteristic length scales of the quantum interference, find the elastic mean-free-paths l_e and compare them to the length scales in the device. In a simple particle-in-a-box picture we can associate oscillations on the gate-voltage axis to the characteristic length scale of the quantum interference, and thus the elastic mean-free-path, using:[34]

$$l_e = \frac{4e}{c_g \Delta V_g} \tag{2}$$

Here ΔV_g is the periodicity in gate-voltage and c_g is the capacitance to the gate per unit length. The capacitance per unit length $c_g = (1.1 \pm 0.2) \times 10^{-10}$ F/m can be taken from the analysis of Fig. 2 where we observed capacitive coupling to the entire channel of the geometrically identical device A.

Following Eq. 2 we convert the dominant gate-voltage spacing in device B to $l_e = 10 \pm 2$ nm and in device C to $l_e = 4 \pm 2$ nm. In device C this yields $l_e < d < L$ (as illustrated in Fig. 2f) at 4 K and a mean-free-path that is on the order of the average spacing of activated phosphorous dopants in the wafer (1.7 nm). This result agrees with our previous mobility measurements on nanowire devices that indicated dominant scattering from neutral impurities – the neutral impurities were likely deactivated dopants in nanowires without gate electrodes and mobilities were improved for lower doping concentrations[35,36]. Considering the prominence of surfaces in such small diameter nanowires this is a result that underpins the effectiveness of the forming gas anneal in reducing the number of interface-trap states as well as the uniformity of the channel walls without significant surface-roughness.

In device B we find $d \lesssim l_e < L < l_\phi$ at 12 mK such that scattering from the radial constraints and impurity-scattering contribute equally to the observed quantum interference as schematically depicted in Fig. 2e. From the activated P concentration in the wafer, the average distance between activated phosphorus dopants can be calculated to be around 3 nm. This suggests that either the doping concentration in the nanowire is reduced due to e.g. surface segregation[37] or that scattering is dominated by deactivated dopants[35,37]. Additionally the activated doping density was determined in the initial 55 nm silicon layer and represents an average over the doping profile – the nanowires are made from only the bottom 10 nm of that layer and might therefore have a different doping concentration. While uncertainties in the doping profile, surface segregation and dielectric effects therefore make a quantitative analysis of doping concentrations difficult, there is a qualitative agreement between the results from the analysis in Fig. 5 and the findings from previous devices since both measurements suggest higher mobility for lower doping concentrations[35]. Furthermore, by reducing the phosphorous concentration by 1 order of magnitude between device C and B, we are able to make the transition between the diffusive transport regime, where the dominant scattering is related to doping density, to the inter-

mediate transport regime, where the contribution of boundary-scattering and impurity-scattering are equal. This provides us with a viable pathway towards a fully ballistic silicon nanowire, either by reducing the channel length to less than 10 nm, or by reducing the doping concentration.

IV. CONCLUSION

In this letter we measure transport in three highly P doped Si nanowires with diameter 8 ± 0.5 nm, length 150 nm and a wrapped-around-gate. One nanowire demonstrates regular Coulomb blockade over a gate-voltage range of 6 V that we attribute to strong electrostatic confinement of electrons into an island that extends along the length of the nanowire and can therefore be used to extract the intrinsic gate capacitance of the nanowire geometry.

In two other devices with larger conductance, we observe quantum interference features that can either originate from random potential fluctuations along the nanowire or transverse modes. We extract an elastic mean-free-path of 4 ± 2 nm in a device fabricated from a wafer with an activated P concentration of $2 \times 10^{20}\,\mathrm{cm}^{-3}$, which is in agreement with dominant scattering from unactivated dopants that was found previously. In a device fabricated from a wafer with a lower P concentration of $4 \times 10^{19}\,\mathrm{cm}^{-3}$, the elastic mean-free-path is 10 ± 2 nm, which is larger than the diameter and therefore allows for significant contribution of radial modes to transport in the nanowire. Temperature dependent measurements in this device show the expected behavior for Universal Conductance Fluctuations and suggest phase-coherence lengths larger than the nanowire length at low temperatures as well as dephasing due to electron-electron interactions at temperatures above 1.9 K. In agreement with previous mobility measurements, these results suggest that the dominant scattering process at low temperatures is impurity scattering rather than scattering due to surface-traps or roughness that is often dominant in nanowire devices[35].

We have demonstrated a junctionless, 1D transistor that could be optimized to reach the ballistic limit for shorter channel-lengths and lower doping-density. The top-down fabrication of our silicon devices is one of the key requirements for CMOS integration, which makes our devices technologically relevant for applications in cryogenic CMOS with minimal heating from transport in ballistic or nearly ballistic channels. Furthermore our devices could represent a platform for quantum electronic devices including charge pumps and charge sensors[38]

ACKNOWLEDGEMENT

The work was funded by the U.K. EPSRC (grants EP/H024107/1, EP/N017188/1 and EP/N003225/1) and DSTL contract 1415NatPhD_59. The authors would like to thank Pascal Gehring and Jonathan Baugh for helpful discussions and the staff of the James Watt Nanofabrication Centre for help and support in undertaking the research.

* jan.mol@materials.ac.uk

[1] Z. Zhong, Y. Fang, W. Lu, and C. M. Lieber, Nano Letters **5**, 1143 (2005).
[2] K. S. Yi, K. Trivedi, H. C. Floresca, H. Yuk, W. Hu, and M. J. Kim, Nano Letters **11**, 5465 (2011).
[3] J. Appenzeller, J. Knoch, M. Bjork, H. Riel, H. Schmid, and W. Riess, IEEE Trans. Elec. Dev. **55**, 2827 (2008).
[4] J.-P. Colinge, C.-W. Lee, A. Afzalian, N. D. Akhavan, R. Yan, I. Ferain, P. Razavi, B. O'Neill, A. Blake, M. White, A.-M. Kelleher, B. McCarthy, and R. Murphy, Nature Nano. **5**, 225 (2010).
[5] S. Nadj-Perge, S. M. Frolov, E. P. A. M. Bakkers, and L. P. Kouwenhoven, Nature **468**, 1084 (2010).
[6] G. Zheng, F. Patolsky, Y. Cui, W. U. Wang, and C. M. Lieber, Nature Biotech. **23**, 1294 (2005).
[7] G. Zheng, X. P. A. Gao, and C. M. Lieber, Nano Letters **10**, 3179 (2010).
[8] H. Park, Y. Dan, K. Seo, Y. J. Yu, P. K. Duane, M. Wober, and K. B. Crozier, Nano Letters **14**, 1804 (2014).
[9] B. Tian, X. Zheng, T. J. Kempa, Y. Fang, N. Yu, G. Yu, J. Huang, and C. M. Lieber, Nature **449**, 885 (2007).
[10] A. I. Boukai, Y. Bunimovich, J. Tahir-Kheli, J. K. Yu, W. A. Goddard, and J. R. Heath, Nature **451**, 168 (2008).
[11] K. J. Kuhn, IEEE Trans. Elec. Dev. **59**, 1813 (2012).
[12] M. M. Mirza, F. J. Schupp, J. A. Mol, D. A. MacLaren, G. A. D. Briggs, and D. J. Paul, Scientific Reports **7**, 3004 (2017).
[13] J. Cao, Q. Wang, and H. Dai, Nature Materials **4**, 745 (2005).
[14] I. Van Weperen, S. R. Plissard, E. P. a. M. Bakkers, S. M. Frolov, and L. P. Kouwenhoven, Nano Letters **13**, 387 (2013).
[15] Y. Wu, J. Xiang, C. Yang, W. Lu, and C. M. Lieber, Nature **430**, 61 (2004).
[16] E. A. Laird, F. Kuemmeth, G. A. Steele, K. Grove-Rasmussen, J. Nygård, K. Flensberg, and L. P. Kouwenhoven, Reviews of Modern Physics **87**, 703 (2015).
[17] W. Lu and C. M. Lieber, Journal of Physics D: Applied Physics **39**, R387 (2006).
[18] A. Dirnaichner, M. del Valle, K. J. G. Götz, F. J. Schupp, N. Paradiso, M. Grifoni, C. Strunk, and A. K. Hüttel, Phys. Rev. Lett. **117**, 166804 (2016).
[19] See Supplementary Material at URL for more information about sample fabrication and Imaging, an estimation of the Fermi-wavelength, a discussion of the power-law dependence of ΔG and additional data..

[20] V. P. Georgiev, M. M. Mirza, A. I. Dochioiu, F. Adamu-Lema, S. M. Amoroso, E. Towie, C. Riddet, D. A. MacLaren, A. Asenov, and D. J. Paul, IEEE Trans. Nano. **16**, 727 (2017).

[21] H. Van Houten, C. W. J. Beenakker, and A. A. M. Staring, "Coulomb-blockade oscillations in semiconductor nanostructures," in *Single Charge Tunneling: Coulomb Blockade Phenomena In Nanostructures*, edited by H. Grabert and M. H. Devoret (Springer US, Boston, MA, 1992) pp. 167–216.

[22] S. J. Shin, C. S. Jung, B. J. Park, T. K. Yoon, J. J. Lee, S. J. Kim, J. B. Choi, Y. Takahashi, and D. G. Hasko, Appl. Phys. Lett. **97**, 103101 (2010).

[23] A. V. Kretinin, R. Popovitz-Biro, D. Mahalu, and H. Shtrikman, Nano Letters **10**, 3439 (2010).

[24] P. Gehring, H. Sadeghi, S. Sangtarash, C. S. Lau, J. Liu, A. Ardavan, J. H. Warner, C. J. Lambert, G. A. D. Briggs, and J. A. Mol, Nano Letters **16**, 4210 (2016).

[25] M. Cahay, M. McLennan, and S. Datta, Phys. Rev. B **37**, 10125 (1988).

[26] M. Elm, P. Uredat, J. Binder, L. Ostheim, M. Schäfer, P. Hille, J. Müßener, J. Schörmann, M. Eickhoff, and P. Klar, Nano Letters **15**, 7822 (2015).

[27] T. Ihn, *Semiconductor Nanostructures* (Oxford University Press, 2009).

[28] H. Yao, H. Y. Günel, C. Blömers, K. Weis, J. Chi, J. G. Lu, J. Liu, D. Grützmacher, and T. Schäpers, Applied Physics Letters **101**, 1 (2012).

[29] P. M. Echternach, M. E. Gershenson, H. M. Bozler, A. L. Bogdanov, and B. Nilsson, Phys. Rev. B **48**, 11516 (1993).

[30] A. T. Tilke, F. C. Simmel, H. Lorenz, R. H. Blick, and J. P. Kotthaus, Phys. Rev. B **68**, 075311 (2003).

[31] W. Lu, J. Xiang, B. P. Timko, Y. Wu, and C. M. Lieber, Proc. Nat. Acad. Sci. USA **102**, 10046 (2005).

[32] C. Beenakker and H. van Houten, in *Solid State Physics*, Vol. 44 (1991) pp. 1–228.

[33] M. Oksanen, A. Uppstu, A. Laitinen, D. J. Cox, M. F. Craciun, S. Russo, A. Harju, and P. Hakonen, Phys. Rev. B **89**, 121414 (2014).

[34] M. J. Biercuk, N. Mason, J. Martin, A. Yacoby, and C. M. Marcus, Phys. Rev. Lett. **94**, 026801 (2005).

[35] M. M. Mirza, D. A. MacLaren, A. Samarelli, B. M. Holmes, H. Zhou, S. Thoms, D. MacIntyre, and D. J. Paul, Nano Letters **14**, 6056 (2014).

[36] M. Diarra, Y. M. Niquet, C. Delerue, and G. Allan, Phys. Rev. B **75**, 1 (2007).

[37] M. T. Bjork, H. Schmid, J. Knoch, H. Riel, and W. Riess, Nature Nano **4**, 103 (2009).

[38] F. J. Schupp, Mat. Sci. Technol. **33**, 944 (2017).

[39] M. M. Mirza, H. P. Zhou, P. Velha, X. Li, K. E. Docherty, A. Samarelli, G. Ternent, and D. J. Paul, J. Vac. Sci. Technol. B **30**, 06FF02 (2012).

[40] C. W. J. Beenakker and H. van Houten, Phys. Rev. B **37**, 6544 (1988).